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**APPLICATION  
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FOR: DRIVE CIRCUIT FOR DRIVING AN IMAGE  
DISPLAY UNIT

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# DRIVE CIRCUIT FOR DRIVING AN IMAGE DISPLAY UNIT

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## BACKGROUND OF THE INVENTION

### (a) Field of the Invention

The present invention relates to a drive circuit for an image display unit and, more particularly, to a drive circuit for driving an image display unit to display thereon multi-level gray-scale digital video data. The present invention also relates to a method for operating such a drive circuit.

### (b) Description of the Prior Art

Fig. 1 illustrates the configuration of a conventional drive circuit for use in an image display unit such as a liquid crystal display (LCD) unit. This drive circuit is used for displaying digital video data of 240 pixels each having six bits, or data of 240 pixels by 6 bits/pixel.

The drive circuit of Fig. 1 includes an 80-bit shift register 901, a data register block 902, a data latch block 903, a gray-scale voltage selector block 904, an output amplifier block 905, and a gray-scale voltage generator 906. Power source voltages VDD1 and VSS1 are supplied to the 80-bit shift register 901, the data register block 902, and the data latch block 903, while power source voltages VDD2 and VSS2 are supplied to the gray-scale voltage selector block 904, and

the output amplifier block 905.

The 80-bit shift register 901 shifts an input pulse in the direction specified by an R/L signal at each cycle of the clock (CLK) signal. More specifically, if the R/L signal indicates the right direction, an STHR signal supplied at the leftmost end of the 80-bit shift register 901 is shifted at each cycle of the CLK signal to output the resulting signal to the data register block 902 as an STHL signal after 80 cycles of the CLK signal. Since the STHR signal includes a single pulse having a width of one clock pulse, pulses are output successively through terminals C1, C2, ... C79, and C80 of the shift register 901 while the STHR signal is being shifted. On the other hand, if the R/L signal indicates the left direction, an STHL signal supplied at the rightmost end of the shift register 901 is shifted at each cycle of the CLK signal to output the resulting signal to the data register block 902 as an STHR signal after 80 cycles of the CLK signal. Since the STHL signal includes also a single pulse having a width of one clock, pulses are output successively through terminals C80, C79, ... C2, and C1 of the shift register 901 while the STHL signal is being shifted.

The data register block 902 has a storage capacity of 1440 bits or a storage capacity for 240 pixels, receives video data D00-D25 for three pixels each including 6 bits in parallel at each cycle of the CLK signal, and successively stores video data in the data register block 902. That is, the video data input to the data register block 902 is successively stored in the data registers of the data register block 902

through terminals C1, C2, ... C79, and C80.

The data latch block 903 latches the 240-pixel video data supplied from the data register block 902 at once when a LATCH signal is active. The data latch block 903 has a capacity of 240-pixel data, and is provided because, while the amplifier block 905 is outputting the video data for one line, the next video data for another line is input to the data register block 902.

The gray-scale voltage generator 906 is configured as shown in Fig. 2, receiving specific gray-scale voltages V0 to V8, providing gray-scale voltage at eight tap points of a resistor ladder or resistor string which divides each adjacent two of the specific gray-scale voltages V0 to V8, and outputting intermediate gray-scale voltages through the tap points of the resistor ladder in association with the specific gray-scale voltages V0 to V8. Accordingly, the gray-scale voltage generator 906 outputs 64 voltage levels. By using a nonlinear adjustment of the levels of the gray-scale voltages V0-V8 in accordance with the characteristics of the LCD unit to be driven, a nonlinear correction can be obtained for the characteristics of the LCD unit with respect to the relation between the voltage and the percent transmission, such as shown in Fig. 3.

Referring to Fig. 4, the gray-scale voltage selector block 904 includes a decoder 904-1 and switches 904-2 for each pixel, the number of switches being equal to the number of gray scale levels to be displayed. The gray-scale voltage selector block 904 selects one voltage out of the 64 voltages, supplied from the gray-scale voltage

generator 906, for the video data of each of the 240 pixels output from the data latch block 903 in accordance with the value of the 6 bits of video data, to output the resulting voltage as an analog signal.

The amplifier block 905 outputs the analog signal of the 240 pixels. These analog signals act as pixel signals of a single line selected by a vertical scan circuit (not shown). In addition, since a plurality of drive circuits for displaying the digital video data are arranged in the horizontal direction, all the pixel signals of the single line are made available simultaneously.

The scheme employed by the drive circuit for displaying digital video data is generally referred to as the "resistor string method". This drive circuit is described in Saito and Kitamura, "Society for Information Display (SID) International Symposium digest of technical papers", Vol. XXVI, pp.257 – 260 (1995). It is to be noted that each gray-scale voltage generator, disposed for a single pixel in the gray-scale voltage selector block 904 described in the literature, includes an enhancement transistor and a depletion transistor, as shown in Fig. 5, and disuses a transistor that is considered necessary to constitute the switch 904-2 shown in Fig. 4.

In the conventional resistor string method described above, although a 6-bit (64-level gray scale) drive circuit can be implemented without a significant problem, an attempt to realize gray-scale levels higher than 64 levels may cause the following problems.

A first problem is that employing a semiconductor integrated circuit implementing the drive circuit may cause the chip to

significantly increase in size. This is because, among others, the number of gray-scale voltage selectors employed in the resistor string method is doubled and doubled as the level of gray scale increases bit by bit. For example, a 64-level gray-scale drive circuit requires 64 gray-scale voltage selectors per one output, whereas a 256-level gray-scale drive circuit requires 256 gray-scale voltage selectors, four times as many as those of the 64-level gray-scale drive circuit. This causes the die area to increase, leading to an increase in its size.

A second problem is that longer time may be required for testing the semiconductor integrated circuit after it is fabricated. The 64-level gray-scale drive circuit has 64 gray-scale voltage selectors per one output, and it is necessary to check the function of all the voltage selectors. Similarly, in the 256-level gray-scale drive circuit, it is necessary to check the function of all the 256 voltage selectors per one output. This may cause the testing time to increase four times, leading to an increase in testing cost.

## SUMMARY OF THE INVENTION

It is therefore an object of the present invention to provide a drive circuit for driving an image display unit, such as a TFT (Thin Film Transistor) LCD unit, to display thereon multi-level gray-scale digital video data, especially such as having gray-scale levels of digital video data higher than eight bits per pixel, to realize reduction of the circuit scale, the die area, and the cost for testing the drive circuit.

The present invention provides a drive circuit for driving a display unit including: a gray-scale level voltage generator for generating a plurality of gray-scale level voltages, the gray-scale voltages corresponding to magnitudes of possible video data in one-to-one correspondence in a non-linear region of characteristic of liquid crystal transmittance and corresponding to magnitudes of possible video data in one-to-n correspondence in a linear region of characteristic of liquid crystal transmittance where n is an integer larger than one; a gray-scale voltage selector block for responding to input video data to select one of the gray-scale level voltages; a judgement section for judging whether a magnitude of an input video data resides within the non-linear region or the linear region to output a judgement signal indicating the non-linear region or the linear region; and an output circuit for responding to the judgement signal to output the one of the gray-scale level voltages selected by the gray-scale voltage selector block when the judgement signal indicates the non-linear region and output one of the gray-scale voltages or an intermediate voltage when the judgement signal indicates the linear region, the intermediate voltage residing between two of adjacent gray-scale voltages.

In accordance with the drive circuit of the present invention, use of the intermediate voltage between adjacent two of the gray-scale voltages in the linear region reduces the number of gray-scale voltages to be generated substantially without degrading the image quality of the image display unit to be driven by the drive circuit, and reduces

the circuit scale of the drive unit and reduces the test procedures for the drive circuit. The intermediate voltage may be preferably obtained by interpolation of the adjacent two of the gray-scale voltages.

5 The above and other objects, features and advantages of the present invention will be more apparent from the following description, referring to the accompanying drawings.

## **BRIEF DESCRIPTION OF THE DRAWINGS**

10 Fig. 1 is a block diagram illustrating the configuration of a conventional drive circuit for displaying multi-level gray-scale digital video data;

Fig. 2 is a circuit diagram illustrating the configuration of a gray-scale voltage generator shown in Fig. 1;

15 Fig. 3 is a graph of a LCD unit showing the relationship between the gray-scale voltage and the optical transmittance of the LCD obtained thereby;

Fig. 4 is a block diagram illustrating the configuration of an example of a gray-scale voltage selector block shown in Fig. 1;

20 Fig. 5 is a block diagram illustrating the configuration of another example of a gray-scale voltage selector block shown in Fig. 1;

25 Fig. 6 is a block diagram illustrating a drive circuit for driving a LCD unit to display thereon multi-level gray-scale digital video data according to a first embodiment of the present invention;



Fig. 7 is a block diagram of the main portion of the drive circuit of Fig. 6.

Fig. 8 is a table showing the relationship between the output voltage and the video data to be received by the drive circuit for displaying multi-level gray-scale digital video data according to the first embodiment of the present invention;

Fig. 9 is a block diagram illustrating the configuration of the output stage amplifier block 104A shown in Fig. 7;

Fig. 10 is a block diagram illustrating the configuration of the least-significant-bit controller 103A shown in Fig. 7;

Fig. 11 is a block diagram illustrating the main portion of a drive circuit for displaying multi-level gray-scale digital video data according to a second embodiment of the present invention;

Fig. 12 is a table showing the relationship between the output voltage and the video data to be received by the drive circuit for displaying multi-level gray-scale digital video data according to the second embodiment of the present invention;

Fig. 13 is a block diagram illustrating the configuration of the output stage amplifier block 104B shown in Fig. 11;

Fig. 14 is a block diagram illustrating the configuration of the least-significant-bit controller 103B shown in Fig. 11; and

Fig. 15 is a circuit diagram illustrating the configuration of a circuit that can be employed in place of a coincidence circuit 301.

## DETAILED DESCRIPTION OF THE PREFERRED

## EMBODIMENTS

Now, the present invention will be described below in more detail with reference to the accompanying drawings in accordance with the preferred embodiments. It is to be noted that similar constituent elements are designated by similar reference numerals or related reference numerals throughout the drawings.

[First embodiment]

Fig. 6 illustrates the configuration of a drive circuit according to the first embodiment of the present invention. The drive circuit of the present embodiment includes an 80-bit shift register 901, a data register block 902, and a data latch block 903, which are similar to those in the conventional drive circuit of Fig. 1. The drive circuit also includes a gray-scale voltage generator 101A, a gray-scale voltage selector block 102A, and an output stage circuit 105A. The gray-scale voltage generator 101A has a circuit configuration which is similar to the circuit configuration of the gray-scale voltage generator 906 shown in Fig. 2. The gray-scale voltage selector block 102A includes a group of 240 gray-scale voltage selectors each having a configuration similar to that shown in Fig. 4.

The output stage circuit 105A includes an amplifier block 104A and a least-significant-bit (LSB) controller 103A, as shown in Fig. 7. The least-significant-bit controller 103A acts as a judgment section which judges whether the magnitude of the video data resides within a non-linear region or a linear region. The output stage amplifier block 104A is somewhat different from the amplifier block 905 shown in Fig.

1.

The gray-scale voltage generator 101A divides input gray-scale reference voltages (VG0 to VGn). In general, to display 64 levels of gray scale data solely by means of the gray-scale voltage selector block 102A, the selector block 102A is provided with 63 resistors to generate 64 distinct voltages. Similarly, to display 256 levels of gray scale data solely by means of the gray-scale voltage selector block 102A, the selector block 102A is generally provided with 255 resistors to generate 256 distinct voltages.

In the present embodiment, however, the gray-scale voltage generator 101A is provided with 159 resistors to generate 160 gray-scale voltages for displaying 256 gray-scale levels on the LCD panel. That is, the gray-scale voltage generator 101A generates 64 gray-scale voltages V0, V1, V2, ... V30, V31, V224, V225, V226, ... V254, and V255 with an 8-bit accuracy in the nonlinear region of characteristic of liquid crystal transmittance with respect to applied voltage. On the other hand, in the linear region of characteristic of liquid crystal transmittance with respect to applied voltage, the gray-scale voltage generator 101A generates 96 gray-scale voltages, V32, V34, ... V220, and V222 with a 7-bit accuracy. Therefore, the gray-scale voltage generator 101A generates 160 different gray-scale voltages in total to output the voltages to the gray-scale voltage selector block 102A.

The gray-scale voltage selector block 102A is configured similarly to the gray-scale voltage selector block in the conventional drive circuit of Fig. 1. As shown in Fig. 8, in accordance with the

values of all of the bits B0-B7 of the digital video data, the gray-scale voltage selector block 102A also selects, as a voltage  $V_{INT}$ , one voltage from the 160 gray-scale voltages that are input from the gray-scale voltage generator 101A. For the magnitudes of digital video data residing within the range of 0 to 31, voltages V0, V1, V2, ... and V31 are selected as voltage  $V_{INT}$ . For the magnitudes of digital video data residing within the range of 32 to 223, voltages V32, V34, V36, ... and V222 are selected as voltage  $V_{INT}$ . For the magnitudes of digital video data residing within the range of 224 to 255, voltages V224, V225, V226, ... and V255 are selected as output voltages  $V_{INT}$ .

In accordance with the value of a control signal 151A input from the least-significant-bit controller 103A, the output stage amplifier block 104A selects and outputs, as an output voltage  $V_{OUT}$ , the voltage  $V_{INT}$  input from the gray-scale voltage selector block 102A or the voltage  $V_{INT}$  added by an offset voltage  $\alpha$ , as detailed below.

An output amplifier in the output stage amplifier block 104A is configured as shown in Fig. 9. The output amplifier has the configuration of a voltage follower modified for controlling the output voltage  $V_{OUT}$  depending on the output signal 151A from the least-significant-bit controller 103A. More specifically, the output amplifier includes a pair of current sources for generating constant currents I1 and I2, a pair of p-ch transistors P1 and P2 acting as a differential pair at a specified situation, a pair of n-ch transistors N1 and N2 forming a current mirror, a p-ch transistor connected in parallel with the p-ch transistor P3, and an n-ch transistor having a gate connected to the

drain of the p-ch transistors P2 and P3, a source connected to the gate of the p-ch transistor P1 and a drain connected to the ground. The gate of p-ch transistor P3 is connected to the output  $V_{INT}$  of the gray-scale voltage selector 102A. The gate of p-ch transistor P2 is connected to  
 5 either the VDD line or the output  $V_{INT}$  of the gray-scale voltage selector 102A through the switch SW1 depending on the output 151A of the least-significant-bit controller 103A. The p-ch transistor P2 has a significantly smaller dimension compared to the p-ch transistor P3.

With p-ch transistor P2 and the switch SW1 being neglected,  
 10 the output amplifier acts as a voltage follower, which allows the output voltage  $V_{OUT}$  to follow the input voltage  $V_{INT}$  of the output amplifier. This state is achieved by connecting the gate of p-ch transistor to the VDD line by the switch SW1. When the gate of p-ch transistor P2 is connected to the output  $V_{INT}$  of the gray-scale voltage selector 102A, the differential pair has some unbalance therebetween  
 15 in the ON-current and allows the output voltage  $V_{OUT}$  to exceed the  $V_{INT}$  by a specified minute voltage or the offset voltage  $\alpha$ . The magnitude of  $\alpha$  is determined at a half of the difference between adjacent two of the gray-scale voltages.

20 If the differential pair are implemented by n-ch transistors, the gate of the parallel transistor is maintained at the ground potential or the output  $V_{INT}$  of the gray-scale voltage selector 102A by the switch SW1.

Referring to Fig. 10, the least-significant-bit controller 103A  
 25 includes a coincidence circuit 301 and an AND gate 302. As can be

seen clearly from Fig. 10, when all of the three significant bits B5-B7 of video data assume “0” or “1”, the coincidence circuit 301 outputs a high level and the least significant bit B0 is disabled, thereby allowing the AND gate 302 to output a low level control signal 151A. On the other hand, when any one of the three significant bits B5-B7 of the video data assumes a value different from those of other two significant bits, the coincidence circuit 301 outputs a low level signal, and thus the AND gate 302 outputs a low level or a high level control signal 151A depending on the least significant bit B0. The switch SW1 couples the gate of p-ch transistor to the output  $V_{INT}$  of the gray-scale voltage selector 102A when the control signal 151A assumes a low level, whereas coupled to the VDD line when the control signal 151A assumes a high level.

Therefore, as shown in Fig. 8, the value of the output voltage  $V_{OUT}$  that is provided by the output stage amplifier block 104A varies depending on the magnitude of the video data. More specifically, for the magnitude of digital video data residing within the range of 0 to 31, the output voltage  $V_{OUT}$  assumes  $V_0$ ,  $V_1$ ,  $V_2$ , ... and  $V_{31}$ . For the magnitude of digital video data residing within the range of 32 to 223, the output voltage  $V_{OUT}$  assumes  $V_{32}$ ,  $V_{32} + \alpha$ ,  $V_{34}$ ,  $V_{34} + \alpha$ , ...  $V_{222}$ ,  $V_{222} + \alpha$ . For the magnitude of digital video data residing within the range of 224 to 255, the output voltage  $V_{OUT}$  assumes  $V_{224}$ ,  $V_{225}$ ,  $V_{226}$ , ... and  $V_{255}$ . It is to be noted that the value of the offset voltage  $\alpha$  is determined about one half the difference between the voltages of  $V_{126}$  and  $V_{128}$ , for example, of a typical LCD panel

by adjusting the size of the p-ch transistor P2, the gate of which is coupled to the  $V_{INT}$  or VDD through the switch SW1, and the p-ch transistor P3 paired therewith. As a concrete example, the offset voltage  $\alpha$  is set within the range from 5mV to 10mV.

5 Of the voltages to be output by the gray-scale voltage generator 101A, the voltages to be output in the nonlinear region may be changed from V32, V34, ... and V222 to V33, V35, ... and V223. In this case, the least-significant-bit controller 103A should be configured differently to supply a different voltage through the switch SW1. This may allow the output stage amplifier block 104A to be adapted such that the voltage  $V_{INT}$  input from the gray-scale voltage selector block 102A remains unchanged as the output voltage  $V_{OUT}$  for the magnitude of digital video data of 33, 35, ... and 223. In addition, the output stage amplifier block 104A may be adapted such that the voltage  $V_{INT}$ , input from the gray-scale voltage selector block 102A, subtracted by the offset voltage is output as the output voltage  $V_{OUT}$  for the magnitude of digital video data of 32, 34, ... and 222.

#### [Second embodiment]

20 Referring to Fig. 11, there is shown the configuration of the main portion of a drive circuit according to a second embodiment of the present invention. The overall configuration is similar to that shown in Fig. 6. A gray-scale voltage generator 101B is similar to the gray-scale voltage generator 906. A group of 240 gray-scale voltage selectors 102B constitutes the gray-scale voltage selector

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block. A least-significant-bit controller 103B is included in the second embodiment. A group of 240 output stage amplifiers constitutes the output stage amplifier block 104B. The output stage amplifier block 104B has a configuration similar to that the output amplifier block 905 shown in Fig. 1 added by resistors and switches.

The gray-scale voltage generator 101B is configured similarly to that shown in Fig. 2 and divides input gray-scale reference voltages ( $V_{G0}$  to  $V_{Gn}$ ). In general, to display 64 levels of gray scale data solely by means of the gray-scale voltage selector 102B, the selector block 102B is provided with 63 resistors to generate 64 distinct voltages. Similarly, to display 256 levels of gray scale data solely by means of the gray-scale voltage selector 102B, the selector block 102B is provided with 255 resistors to generate 256 distinct voltages.

In the present embodiment, however, the gray-scale voltage generator 101B is provided with 111 resistors to generate 112 voltages. More specifically, the gray-scale voltage generator 101B generates 64 gray-scale voltages  $V_0, V_1, V_2, \dots, V_{30}, V_{31}, V_{224}, V_{225}, V_{226}, \dots, V_{254}$ , and  $V_{255}$  with an 8-bit accuracy in the nonlinear region of characteristic of liquid crystal transmittance with respect to applied voltage. On the other hand, in the linear region of characteristic of liquid crystal transmittance with respect to applied voltage, the gray-scale voltage generator 101B generates 48 gray-scale voltages  $V_{32}, V_{36}, \dots, V_{216}$ , and  $V_{220}$  with a 6-bit accuracy. Therefore, the gray-scale voltage generator 101B generates 112 different gray-scale voltages in total to output the voltages to the gray-scale voltage



selector block 102B.

The gray-scale voltage selector block 102B is configured similarly to a combination of two of the conventional gray-scale voltage selector block shown in Figs. 4 and 5. As shown in Fig. 12, in accordance with the values of all of the bits B0-B7 of the digital video data, the gray-scale voltage selector block 102B also selects, as voltages  $V_U$ ,  $V_D$ , two adjacent voltages from the 112 gray-scale voltages that are input from the gray-scale voltage generator 101B.

More specifically, for the magnitude of digital video data residing within the range of 0 to 31, voltages  $V_0$ ,  $V_1$ ,  $V_2$ , ... and  $V_{31}$  are selected as voltage  $V_D$ . For the magnitude of digital video data residing within the range of 32 to 223, voltages  $V_{32}$ ,  $V_{36}$ ,  $V_{40}$ , ... and  $V_{220}$  are selected as voltage  $V_D$ . For the magnitude of digital video data residing within the range of 224 to 255, voltages  $V_{224}$ ,  $V_{225}$ ,  $V_{226}$ , ... and  $V_{255}$  are selected as voltage  $V_D$ . Furthermore, for the magnitude of digital video data residing within the range of 0 to 31, voltages  $V_1$ ,  $V_2$ ,  $V_3$ , ... and  $V_{32}$  are selected as voltage  $V_U$ . For the magnitude of digital video data residing within the range of 32 to 223, voltages  $V_{36}$ ,  $V_{40}$ ,  $V_{44}$ , ... and  $V_{224}$  are selected as voltage  $V_U$ . For the magnitude of digital video data residing within the range of 224 to 255, voltages  $V_{225}$ ,  $V_{226}$ ,  $V_{227}$ , ... and  $V_{255}$  are selected as voltage  $V_D$ .

In accordance with the value of a control signal 151B input from the least-significant-bit controller 103B, the output stage amplifier block 104B outputs, as output voltage  $V_{OUT}$ , the voltage

generated in accordance with the voltages  $V_U$ ,  $V_D$  that are input from the gray-scale voltage selector block 102B.

As shown in Fig. 13, the output stage amplifier block 104B includes four resistors for dividing the voltage between  $V_U$  and  $V_D$ , switches SW2 to SW5 for selecting a voltage at any one of the tap points of the resistors or the voltage  $V_D$ , and a buffer amplifier A1 for reducing the output impedance of the switches SW2 to SW5. The switches SW2 to SW5 are controlled by the control signal 151B that is output from the least-significant-bit controller 103B.

When the control signal 151B selects the switch SW2, the voltage  $V_{OUT}$  becomes equal to the voltage  $V_D$ . When the control signal 151B selects the switch SW3, the voltage  $V_{OUT}$  becomes equal to  $(3/4)V_D + (1/4)V_U$ . When the control signal 151B selects the switch SW4, the voltage  $V_{OUT}$  becomes equal to  $(2/4)V_D + (2/4)V_U$ . When the control signal 151B selects the switch SW5, the voltage  $V_{OUT}$  becomes equal to  $(1/4)V_D + (3/4)V_U$ .

As shown in Fig. 14, the least-significant-bit controller 103B includes a coincidence circuit 301, a 2-to-4 line decoder 303, an OR gate 304, and AND gates 305 to 307. The output terminal of the OR gate 304 is connected to a control terminal C2 of the switch SW2. The output terminal of the AND gate 305 is connected to a control terminal C3 of the switch SW3. The output terminal of the AND gate 306 is connected to a control terminal C4 of the switch SW4. The output terminal of the AND gate 307 is connected to a control terminal C5 of the switch SW5.

As can be seen clearly from Fig. 14, when all the values of the three significant bits B5-B7 of video data assume "0" or "1", the coincidence circuit 301 outputs a high level signal, thereby causing the OR gate 304 to output a high level signal and the AND gates 305-307 to output a low level signal. Therefore, at this time, of the switches SW2 to SW5, only the switch SW2 is turned on. On the other hand, when any one of the three significant bits B5-B7 of the video data assumes a value different from the values of other two significant bits, the coincidence circuit 301 outputs a low level signal. Then, the OR gate 304 and the AND gates 305-307 output a low level or a high level control signal 151B depending on the value of the less significant two bits B0 and B1. Therefore, at this time, in accordance with the value of the less significant two bits B0 and B1 of the video data, one of the switches SW2 to SW5 is turned on and other switches are turned off.

Therefore, as shown in Fig. 12, the value of the output voltage  $V_{OUT}$  that is provided from the output stage amplifier block 104B varies depending on the value of video data. That is, for the magnitude of digital video data residing within the range of 0 to 31, the output voltage  $V_{OUT}$  assumes  $V_0, V_1, V_2, \dots$  and  $V_{31}$ . For the magnitude of digital video data residing within the range of 32 to 223, the output voltage  $V_{OUT}$  assumes  $V_{32}, (3/4)V_{32} + (1/4)V_{36}, (2/4)V_{32} + (2/4)V_{36}, (1/4)V_{32} + (3/4)V_{36}, V_{36}, \dots V_{220}, (3/4)V_{220} + (1/4)V_{224}, (2/4)V_{220} + (2/4)V_{224},$  and  $(1/4)V_{220} + (3/4)V_{224}$ . For the magnitude of digital video data residing within the range of 224 to

255, the output voltage  $V_{OUT}$  assumes  $V_{224}$ ,  $V_{225}$ ,  $V_{226}$ , ... and  $V_{255}$ .

Other examples of the output circuit that can be incorporated into the output stage amplifier block include a D/A converter that can generate, from a plurality of reference voltages, a plurality of voltages greater in number than the reference voltages such as by a switched capacitor method employing capacitors or a R-2R method employing resistors.

It is to be noted that, in the first and second embodiments, the least-significant-bit controller 103A or 103B determines whether or not a gray-scale voltage to be displayed is within a linear region, using the coincidence circuit 301 to determine whether or not all the three significant bits of video data coincide with each other. The present invention, however, is not limited thereto. For example, as shown in Fig. 15, instead of the coincidence circuit 301, it is possible to employ a circuit including two comparators 321 and 322 and an OR gate 323 for receiving the outputs of these comparators in order to set given threshold values TH1 and TH2 indicative of the boundary between the linear and nonlinear regions.

It is also possible to combine the following components in order to further reduce the scale of the gray-scale voltage selector block. That is,

- (1) The gray-scale voltage selector block 102A,
- (2) A decoder that replaces the 2-to-4 line decoder 303 to provide one to four high level outputs in accordance with the value of the

bits B0 and B1, and the OR gate 304 or the least-significant-bit controller 103B with the output thereof eliminated, and

- (3) The switch SW1, and the output stage amplifier block 104A having three pairs of transistors, the gates of which are connected to the switch SW1.

As described above, according to the preferred embodiments of the present invention, in the linear region of characteristic of liquid crystal transmittance with respect to applied voltage, the gray-scale voltage selector block selects one or two voltages in accordance with the value of the significant bits of video data. By using the selected voltages, further divided voltages are generated in accordance with the value of the remaining less significant bits of all the bits of the video data. This makes it possible to significantly reduce the scale of the gray-scale voltage selector block. On the other hand, in the nonlinear region of characteristic of liquid crystal transmittance with respect to applied voltage, a difference between gray-scale voltages (a difference in voltage to obtain the same difference in gray scale) is greater than in the linear region and not even. However, the nonlinear region is determined in accordance with part of the significant bits to generate and then select gray-scale voltages with an 8-bit accuracy. Thus, this makes it possible to display, on a liquid crystal display panel, an image with properly expressed levels of gray scale. It is also possible to implement, for example, a full-color display of 16,770,000 colors by using a liquid crystal panel of three primary colors and three drive circuit systems when employed

accordingly.

Furthermore, according to the embodiments, the scale of the gray-scale voltage selector block can be reduced. Even with an increase in scale of the output circuit, it is possible to reduce the entire scale of the drive circuit.

The conventional 8-bit resistor string method requires that the gray-scale voltage selector blocks be provided per one output with a decoder compliant with 256 levels of gray scale and 256 switches. In contrast, the first embodiment requires that the gray-scale voltage selector blocks be provided per one output only with a decoder compliant with 160 levels of gray scale and 160 switches. Furthermore, the second embodiment requires that the gray-scale voltage selector blocks be provided per one output only with two sets of a decoder compliant with 112 levels of gray scale and 112 switches.

With the reduced number of gray scale levels to be output by the gray-scale voltage selector blocks, the number of gray scale levels to be tested is also reduced. This makes it possible to carry out the test of the chip in a shorter time and thereby reduce the cost of the chip. It is not necessary to test the output circuit on all levels of gray scale, and instead, it is sufficient to test all the combinations of the control signals.

Since the above embodiments are described only for examples, the present invention is not limited to the above embodiments and various modifications or alterations can be easily made therefrom by those skilled in the art without departing from the scope of the present

invention.

1. The invention relates to a method of determining the position of a point in a 3D space by means of a camera and a sensor.